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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/760,309	01/21/2004	Tsang-Chi Kan	BHT-3111-404	1537

7590 09/20/2006

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EXAMINER	
DOAN, NGHIA M	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 09/20/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/760,309	KAN ET AL.	
	Examiner	Art Unit	
	Nghia M. Doan	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 May 2006 and 01 September 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) *1-6* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *7-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Responsive communication application 10/760,309 filed on 01/1/2004, Applicant Amended filed on 05/22/2006, and Response to election/restriction filed on 09/01/2006, claims 1-12 are pending.

Claims 7-11 have been amended.

Claims 1-6 have been withdrawn from election/restriction required.

Claim 12 has been added.

2. Claims 7-12 are to be examining in this office action and Applicant is advised to cancel non-elected claims (claims 1-6) in the next communication.

3. Applicant's arguments with respect to claim 7 have been considered but are moot in view of the new ground(s) of rejection.

Claim Objections

4. Claim 7 is objected to because of the following informalities:

As per line 15, recited " *upper metal layer being connected to fewer than all of the pluralities of circuit passageways*", is unclear limitations that need to be clarified.

As per line 17, recited *"testing said circuit elements to identify a desired modification"*, that is missing a functional/ structural of relationship between IC routing layout and the step of testing. Moreover, what kind/type the test to be performed? How to identify a desired modification?

Appropriate correction is required.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 7-12 are rejected under 35 U.S.C. 102(b) as being anticipated by Fukasawa (US PG Pub. 20020074660).

7. With respect to claim 7, Fukasawa discloses an integrated circuit (IC) layout design method utilized for connection of elements in a standard cell *(figure 9)*, wherein said IC comprises a substrate *(silicon bulk layer)(figure 9, element [33])*, said substrate further including pluralities of circuit elements *(MOS transistor gate)(figure 9, elements MOS transistor gates [22])*; and m metal layers disposed on said substrate *(four metal layers)(figure 9, elements [23-26])*, which are utilized as connection layout for circuit elements *(figure 9, elements [SVIA])*, wherein each metal layer further including an isolation layer for electrical isolation among said metal layers said IC layout design *(figure 9, element [31's])* method comprising the following steps:

arranging pluralities of circuit passageway *(figure 9, elements [27-30])* at one terminal of a circuit element, said pluralities of circuit passageway extends from said substrate through at least two metal layers *(figure 9, element [SVIA])*;

connecting pluralities of lines which are required to be electrically connected to said terminal, to said terminal by connecting said lines to said circuit passageways *(figure 9, elements SVIA [27-30] and terminal [22])*;

forming an upper metal layer overlying the pluralities of circuit passageways, said upper metal layer being connected to fewer than all of the pluralities of circuit passageways *(figures 5B, and 7B with upper metal layer [M4] as show in different view of figure 9)*;

testing *(checking)* said circuit element to identify a desired modification *(to meet the conditions of the design standards) (page 5, paragraph [0055], lines 1-7 and figures 8, step [S3])*; and

modifying *(deleting and updating list of SVIA)*said circuit element by connecting said upper metal layer to one of said pluralities of circuit passageways *(page 5, paragraph [0055], lines 13-36 and figures 8, steps [S3-S6])*.

8. With respect to claim 8, Fukasawa discloses the IC layout design method of claim 7, wherein at least one of pluralities of said circuit passageways connects through two metal layers *(figure 9, vias [27,28] connect through two metal layers [23,24])*.

9. With respect to claim 9, Fukasawa discloses the IC layout design method of claim 7, wherein at least one of pluralities of said circuit passageways connects through three metal layers *(figure 9, vias [27,28,29] connect through three metal layers [23,24,25])*.

10. With respect to claim 10, Fukasawa discloses the IC layout design method of claim 7, wherein said standard cell is connected to an intellectual property element *(SVIA portions wired using EDA tools have structure as shown in figure 11)(page 1, paragraph [0007])*.

11. With respect to claim 11, Fukasawa discloses the IC layout design method of claim 7, wherein said standard cell is connected to an intellectual property element library *(SVIA portions wired using EDA tools have structure as shown in figure 11)(page 1, paragraphs [0006-0007])*.

12. With respect to claim 12, Fukasawa discloses the IC layout design method claim 7, further comprising reserving said upper metal layer exclusively for modification during a subsequent reworking of said circuit element *(pages 5-6, paragraphs [0055 and 0063])*.

Conclusion

13. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nghia M. Doan whose telephone number is 571-272-5973. The examiner can normally be reached on 8:30-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571-272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Nghia M. Doan
Patent Examiner
AU 2825
NMD

PAUL DINH
PRIMARY EXAMINER